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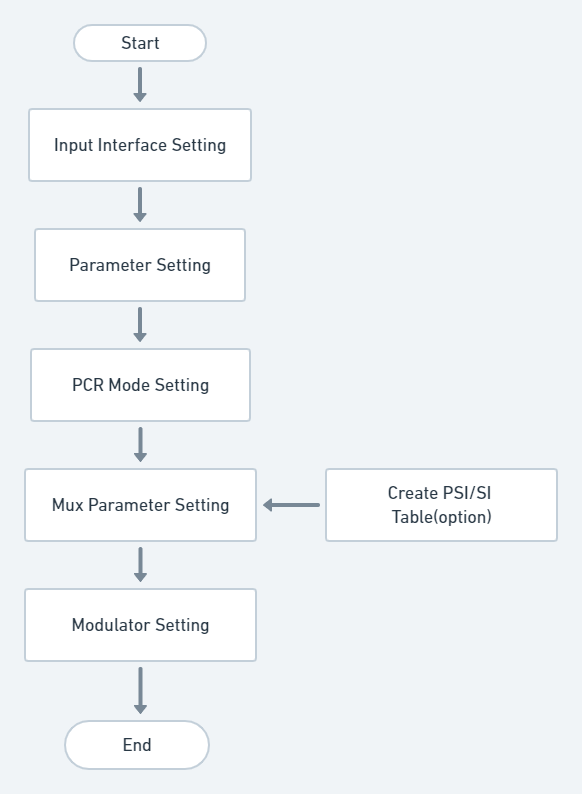
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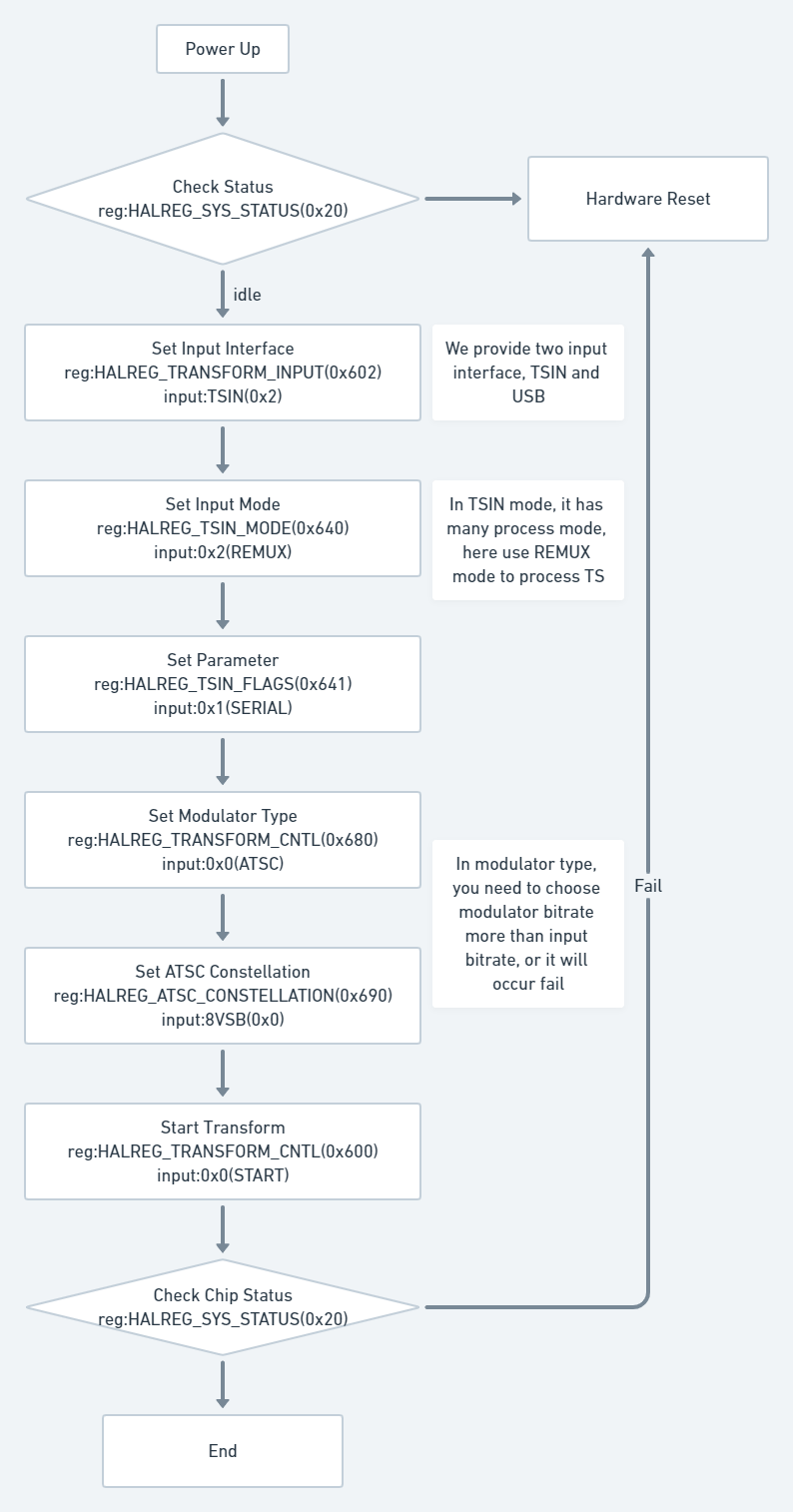
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## 1.System Process

### 1.1 Process Overview



### 1.2 Process of Chip



## 2. Status Registers(BASE)

The BASE registers are basic information register sets for VATek chips. Base register sets help developer to understand chip basic information and real-time status, which includes chip status, chip ID, supported functions and information lists and error code as well.

### 2.1 System Status

**0x20 - HALREG\_SYS\_STATUS\_0:** System Status Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0-7 | R | 0xFF000001 | SYS\_STATUS\_IDLE |
| R | 0xFF000002 | SYS\_STATUS\_RUN |
| R | 0xFF000080 | SYS\_STATUS\_ERRTAG |
| R | 0xFF000085 | SYS\_STATUS\_LOADER FAIL |
| R | 0xFF000086 | SYS\_STATUS\_SERVICE\_FAIL |
| R | 0xFF000088 | SYS\_STATUS\_EXCEPTION\_FAIL |
| R | 0xFF00008E | SYS\_STATUS\_BADSTATUS |
| R | 0xFF00008F | SYS\_STATUS\_UNKNOWN\_FAIL |
| 8-23 | -- | Reserved | Reserved |
| 24-31 | R | 0xFF000000 | SYS\_STATUS\_TAG |

**Description**

This register use to read chip status, when reset chip and power up, chip status will be SYS\_STATUS\_IDLE, if the service is running, status will be SYS\_STATUS\_RUN,

**0x23 - HALREG\_SYS\_ERRCODE:** System Error Code

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0-31 | R | 0x80000001 | SYS\_ERRCODE\_INIT |
| R | 0x80010001 | LOADER\_ERRCODE\_NOAPP |
| R | 0x80010002 | LOADER\_ERRCODE\_CRC32 |
| R | 0x80010003 | LOADER\_ERRCODE\_HW |
| R | 0x80020001 | SERVICE\_INIT\_FAIL |
| R | 0x80020002 | SERVICE\_HW\_FAIL |

**Description**

This register use to show error code from chip, if firmware download fail in chip, the error code will happen.

**0x24 - HALREG\_CHIP\_ID**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0-31 | R | 0x00010100 | HAL\_CHIPID\_A1 |
| R | 0x00010300 | HAL\_CHIPID\_A3 |
| R | 0x00020100 | HAL\_CHIPID\_B1 |
| R | 0x00020200 | HAL\_CHIPID\_B2 |
| R | 0x00020201 | HAL\_CHIPID\_B2\_PLUS |
| R | 0x00020300 | HAL\_CHIPID\_B3 |
| R | 0x00020301 | HAL\_CHIPID\_B3\_PLUS |

**Description**

This register will show what chip is connecting,

**0x25 - HALREG\_FW\_VER**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | -- |  |

**Description**

This register shows firmware version, version number made by create date of firmware(.v2app) in hex.

**0x26 - HALREG\_SERVICE\_MODE:** Chip Service Mode

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | 0xFF000001 | SERVICE\_TAG\_RESCUE |
| R | 0xF8000001 | SERVICE\_TAG\_BROADCAST |
| R | 0xF8000002 | SERVICE\_TAG\_TRANSFORM |

**Description**

This register shows chip services, we provide two services base on different chip series, and rescue mode is use to update firmware, you can you romtool to update firmware or use HAL regiseter to write v2img in chip.

**0x27 - HALREG\_PERIPHERAL\_EN:** Peripheral Chip ID

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R | 0x000000FF | PERIPHERAL\_RF\_MASK |
| R | 0x00000002 | PERIPHERAL\_FINTEKR2 |
| R | 0x00FF0000 | PERIPHERAL\_VIDEO\_MASK |
| R | 0x00010000 | PERIPHERAL\_EP9555E |

**Description**

This register shows what peripheral device we connect with chip.

**0x28 -** **HALREG\_INPUT\_SUPPORT:** Supported Functions

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000001 | INPUT\_EN\_TEST |
| 1 | R | 0x00000002 | INPUT\_EN\_USB |
| 2 | R | 0x00000004 | INPUT\_EN\_TS |
| 3 | R | 0x00000008 | INPUT\_EN\_ENC |
| 4 | R | 0x00000010 | VENC\_EN\_MPEG2 |
| 5 | R | 0x00000020 | VENC\_EN\_H264 |
| 7 | -- | Reserved |  |
| 8 | R | 0x00000100 | VENC\_EN\_FULLHD |
| 9 ~11 | -- | Reserved |  |
| 12 | R | 0x00001000 | AENC\_EN\_MP1\_L2 |
| 13 | R | 0x00002000 | AENC\_EN\_AAC\_LC\_ADTS |
| 14 | R | 0x00004000 | AENC\_EN\_AC\_3 |
| 15 | R | 0x00008000 | AENC\_EN\_AAC\_LC\_LATM |
| 16 | R | 0x00010000 | TSIN\_EN\_BYPASS |
| 17 | R | 0x00020000 | TSIN\_EN\_TSSMOOTH |
| 18 | R | 0x00040000 | TSIN\_EN\_TSREMUX |
| 19 | R | 0x00070000 | TSIN\_EN\_ALL |
| 20 | R | 0x00100000 | TEST\_EN\_HW |
| 21 | R | 0x00200000 | TEST\_EN\_REMUX |
| 22 | R | 0x00300000 | TEST\_EN\_ALL |
| 23-31 | -- | Reserved | Reserved |

**Description**

This register shows many input we support, we support different input interfaced, and TS input interface has many process mode, BYPASS, TSSMOOTH, TSREMUX,

**0x29 - HALREG\_OUTPUT\_SUPPORT:** Supported Output Functions

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000001 | OUTPUT\_EN\_MOD |
| 2 | R | 0x00000004 | OUTPUT\_EN\_TS |
| 3 | R | 0x00000008 | OUTPUT\_EN\_USB |
| 4-6 | -- | Reserved |  |
| 8 | R | 0x00000100 | MOD\_EN\_DVB\_T |
| 7 | R | 0x00000200 | MOD\_EN\_J83\_A |
| 9 | R | 0x00000400 | MOD\_EN\_ATSC |
| 10 | R | 0x00000800 | MOD\_EN\_J83\_B |
| 11 | R | 0x00001000 | MOD\_EN\_DTMB |
| 12 | R | 0x00002000 | MOD\_EN\_ISDB\_T |
| 13 | R | 0x00004000 | MOD\_EN\_J83\_C |
| 14 | R | 0x00008000 | MOD\_EN\_DVB\_T2 |
| 15 | R | 0x00005F00 | MOD\_EN\_BASE |
| 16 | R | 0x01000000 | DVB\_T2\_EN\_FFT32K |
| 17-31 | -- | Reserved | Reserved |

**Description**

This register shows output we support, we have many modulators you can choose based on different country.

### 2.2 Transform Status

**0x620 - HALREG\_BCINFO\_STREAM:** Show the setting value of HALREG\_BROADCAST\_STREAM.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | R | 0x00000000 | STREAM\_TESTMODE |
| R | 0x00000001 | STREAM\_USB |
| R | 0x00000002 | STREAM\_TSIN |
| R | 0x00000003 | STREAM\_ENCODER |
| 3~31 |  | Reserved |  |

**Description**

This register use to read what input interface using now,

**0x621 - HALREG\_BCINFO\_OUTPUT:** Show the setting value of HALREG\_BROADCAST\_OUTPUT.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | R | 0x00000000 | OUTPUT\_MODULATOR |
| 1~31 |  | Reserved |  |

**Description**

This register use to read output mode, we provide modulator mode to be output, you can choose different modulator type.

**0x622 - HALREG\_BCINFO\_MODRATE**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**Description**

This register use to read real output bitrate of modulator, bitrate size base on different modulator type.

**0x623 - HALREG\_BCINFO\_MUXRATE:** Show Bitrate of MUX.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**Description**

This register use to read MUXER bitrate.

**0x624 - HALREG\_BCINFO\_STATUS**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | R | 0x00000000 | BCSTATUS\_IDLE |
| R | 0x00000001 | BCSTATUS\_WAIT\_SOURCE |
| R | 0x00000002 | BCSTATUS\_BROADCAST |
| R | 0x00000003 | BCSTATUS\_FINISH |
| 2~31 |  | Reserved |  |
| 32 | R | 0x80000000 | BCSTATUS\_FAIL\_UNKNOWN |
| R | 0x80000001 | BCSTATUS\_FAIL\_SOURCE |
| R | 0x80000002 | BCSTATUS\_FAIL\_TIMEOUT |
| R | 0x80000003 | BCSTATUS\_FAIL\_CODECDROP |
| R | 0x80000004 | BCSTATUS\_FAIL\_BUFFER |
| R | 0x80000005 | BCSTATUS\_FAIL\_MUXER |
| R | 0x80000006 | BCSTATUS\_FAIL\_ENCODE |
| R | 0x80000007 | BCSTATUS\_FAIL\_MEDIA |
| R | 0x80000008 | BCSTATUS\_FAIL\_DEMUX |

**Description**

This register use to read broadcast status.

**0x625 - HALREG\_BCINFO\_CURRATE:** Show real bitrate of MUX.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

**Description**

This register use to read current bitrate of MUXER

## 3. Transform Input Registers

Broadcaster registers are the main switches to activate / deactivate modulator, RF mixer. The operating status indicators are also in the register set.

### 3.1 Transform Control

**0x602 - HALREG\_TRANSFORM\_INPUT:** Transform input Select

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | STREAM\_NULL |
| W | 0x00000001 | STREAM\_USB |
| W | 0x00000002 | STREAM\_TSIN |
| W | 0x00000003 | STREAM\_ENCODER |
| W | 0x00001000 | STREAM\_SINE |
| W | 0x00001001 | STREAM\_TEST |

### 3.2 A USB Mode Parameter

**0x640 - HALREG\_USB\_INPUT\_MODE:** USB MODE Control

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W |  |  |
| 1-31 | -- | Reserved | Reserved |

**0x641 - HALREG\_USB\_STREAM\_FLAGS:** USB MODE FLAGS

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W |  |  |
| 1-31 | -- | Reserved | Reserved |

**0x642 - HALREG\_USB\_PCR\_MODE:** PCR MODE IN USB MODE

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W |  |  |
| 1-31 | -- | Reserved | Reserved |

**0x643 - HALREG\_USB\_ADJUST\_TICK:** USB MODE ADJUST TICK SET

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W |  |  |
| 1-31 | -- | Reserved | Reserved |

### 3-2 B TSIN Mode

**0x640 - HALREG\_TSIN\_MODE:** TS mode select (Pure Modulator Only)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
|  | W | 0x00000001 | STREAM\_MODE\_SMOOTH |
| W | 0x00000002 | STREAM\_MODE\_REMUX |
| W | 0x00000003 | STREAM\_MODE\_PASSTHROUGH |
| 2-31 | -- | Reserved | Reserved |

**0x641 - HALREG\_TSIN\_FLAGS:** TS interface function flags

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000001 | TS\_PIN\_SERIAL |
| 1 | W | 0x00000002 | TS\_PIN\_NEGATIVE\_CLK |
| 2 | W | 0x00000004 | TS\_PIN\_NEGATIVE\_VALID |
| 3 | W | 0x00000008 | TS\_PIN\_NEGATIVE\_SYNC |
| 4-31 | -- | Reserved | Reserved |

**0x642 – HALREG\_TSIN\_PCR\_MODE:** TS PCR Mode

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | PCR\_MODE\_DISABLE |
| 1 | W | 0x00000001 | PCR\_MODE\_ADJUST |
| 2 | W | 0x00000002 | PCR\_MODE\_RETAG |

## 4. MUX Registers

Regarding to the information of PSI/SI MUX insertion refers to psi insertion porting guide.

### 4.1 Mux Related Settings

**0x610 - HALREG\_MUX\_PCR\_PID:** Register for Writing PCR PID

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x611 - HALREG\_MUX\_PADDING\_PID:** Register for Writing Padding PID

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x612 - HALREG\_BITRATE:** Register for Writing Bitrate Limitation

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x2000 - HALREG\_MUXPSI\_MODE:** Produce Mode of PSI

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | MUX\_PURE |
| 3 | W | 0x00000003 | MUX\_DEFSPEC |
| 4~31 |  | Reversed |  |

## 5. PSI Register

### 5.1 Playload Buffer Register

**0x2100 - HALRANGE\_PLAYLOAD\_START:** register of register PSI/SI table start tag, it’s start at 0x2100.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x3000 - HALRANGE\_PLAYLOAD\_END:** register of register PSI/SI table end tag, it’s end at 0x3000

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

### 5.2 PSI Pure Mode

Please follow [appendix A](#_A._Register_PSI/SI)

**0x00 - HALOF\_RAWPSI\_TAG:** start and end tag in PSI PURE mode, you need to use start tag when writing new PSI table, and use end tag after finishing table.

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W | 0xFF070600 | RAWPSI\_EN\_TAG |
| W | 0xFF0706FF | RAWPSI\_EN\_ENDTAG |

**0x01 - HALOF\_RAWPSI\_INTERVAL:** PSI Table Interval Time (ms)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x02 - HALOF\_RAWPSI\_PACKETS:** PSI Table packet size

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x03 – HALOF\_RAWPSI\_DATA:** write PSI table data continuously

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

### 5.3 Private PSI table

Please follow [appendix B](#_B._Insert_PSI/SI)

Private PSI table is the way in PURE mode, it’s only can be inserted table after chip start broadcast, but private PSI provide dynamically modify and insert table.

**0x639 – HALREG\_PRIVATE\_START:** private stream playload start address

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x63A – HALREG\_PRIVATE\_END:** private stream playload end address

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x063B – HALREG\_PRIVATE\_CNTL:** private stream control

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x80000000 | PRIVATE\_EN\_CONTINUE |
| 1 | W | 0x00000001 | PRIVATE\_EN\_TIMES |
| 2~31 | W |  |  |

**Description**

* PRIVATE\_EN\_CONTINUE: when write and read pointer are not equal, user can use this flag to send PSI table to chip.
* PRIVATE\_EN\_TIMES: set PRIVATE\_EN\_TIMES can insert table one time after broadcast start.

**0x63C – HALREG\_PRIVATE\_WPTR:** Private stream write pointer (update by user)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | W |  |  |

**0x63D – HALREG\_PRIVATE\_RPTR:** private stream read pointer (update by hardware)

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~31 | R |  |  |

## 6. Modulator Register

### 6.1 Modulator Related Settings

**0x601 - HALREG\_TRANSFORM\_MODE:** Transform Mode Select

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
|  | W | 0x00000005 | TRANSFORM\_BROADCAST |

**0x680 - HALREG\_MODULATOR:** Modulation Standard Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~3 | W | 0x00000000 | MOD\_DVB\_T |
| W | 0x00000001 | MOD\_J83A |
| W | 0x00000002 | MOD\_ATSC |
| W | 0x00000003 | MOD\_J83B |
| W | 0x00000004 | MOD\_DTMB |
| W | 0x00000005 | MOD\_ISDB\_T |
| W | 0x00000006 | MOD\_J83C |
| W | 0x00000007 | MOD\_DVB\_T2 |
| 4~31 |  | Reserved |  |

**0x681 - HALREG\_MOD\_IFMODE:** Modulation Switch Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000001 | IFMODE\_DISABLE |
| W | 0x00000003 | IFMODE\_IQ\_OFFSET |
| 2~31 |  | Reserved |  |

**0x682 - HALREG\_MOD\_IFFREQ:** Offset Setting Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
|  | W |  |  |

**0x683 - HALREG\_MOD\_DACGAIN:** DAC Gain Setting Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
|  | W |  |  |

**0x684 - HALREG\_MOD\_BW\_SB:** Modulator Bandwidth or Symbol Rate Setting Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
|  | W |  |  |

### 6.2 DVB-T Settings

**0x690 - HALREG\_DVB\_T\_CONSTELLATION:** DVB-T Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | DVB\_T\_QPSK |
| 1 | W | 0x00000002 | DVB\_T\_QAM16 |
| 2 | W | 0x00000004 | DVB\_T\_QAM64 |
| 3~31 |  | Reserved | -- |

**0x691 - HALREG\_DVB\_T\_FFT:** DVB-T Carrier Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DVB\_T\_FFT2K |
| W | 0x00000001 | DVB\_T\_FFT8K |
| W | 0x00000002 | DVB\_T\_FFT4K |
| 2~31 |  | Reserved | -- |

**0x692 - HALREG\_DVB\_T\_GUARDINTERVAL:** DVB-T Guard Interval Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DVB\_T\_GI\_1\_32 |
| W | 0x00000001 | DVB\_T\_GI\_1\_16 |
| W | 0x00000002 | DVB\_T\_GI\_1\_8 |
| W | 0x00000003 | DVB\_T\_GI\_1\_4 |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_DVB\_T\_CODERATE:** DVB-T Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | DVB\_T\_CODERATE\_1\_2 |
| W | 0x00000001 | DVB\_T\_CODERATE\_2\_3 |
| W | 0x00000002 | DVB\_T\_CODERATE\_3\_4 |
| W | 0x00000003 | DVB\_T\_CODERATE\_5\_6 |
| W | 0x00000004 | DVB\_T\_CODERATE\_7\_8 |
| 3~31 |  | Reserved | -- |

### 6.3 DVB-C (J83A) Settings

**0x690 - HALREG\_J83A\_CONSTELLATION:** DVB-C (J83.A) Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | J83A\_QAM16 |
| W | 0x00000001 | J83A\_QAM32 |
| W | 0x00000002 | J83A\_QAM64 |
| W | 0x00000003 | J83A\_QAM128 |
| W | 0x00000004 | J83A\_QAM\_256 |
| 3~31 |  | Reserved | -- |

### 6.4 ATSC (8VSB) Settings

**0x690 - HALREG\_ATSC\_ CONSTELLATION:** ATSC (8VSB) Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | ATSC\_8VSB |
| 1~31 |  | Reserved | -- |

### 6.5 Clear QAM (J83.B) Settings

**0x690 - HALREG\_J83B\_CONSTELLATION:** Clear QAM(J83B) Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000001 | J83B\_QAM64 |
| W | 0x00000003 | J83B\_QAM128 |
| 2~31 |  | Reserved | -- |

### 6.6 DTMB Settings

**0x690 - HALREG\_DTMB\_CONSTELLATION:** DTMB Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | DTMB\_QPSK |
| W | 0x00000001 | DTMB\_QAM16 |
| W | 0x00000002 | DTMB\_QAM64 |
| W | 0x00000004 | DTMB\_QAM32 |
| 3~31 |  | Reserved | -- |

**0x691 - HALREG\_DTMB\_TIME\_INTERLEAVED:** DTMB Time Interleaved Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DTMB\_TI\_DISABLE |
| W | 0x00000001 | Reserved |
| W | 0x00000002 | DTMB\_TI\_240 |
| W | 0x00000003 | DTMB\_TI\_720 |
| 2~31 |  | Reserved | -- |

**0x692 - HALREG\_DTMB\_CODERATE:** DTMB Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DTMB\_CODERATE\_0\_4 |
| W | 0x00000001 | DTMB\_CODERATE\_0\_6 |
| W | 0x00000002 | DTMB\_CODERATE\_0\_8 |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_DTMB\_CARRIERMODE:** DTMB Carrier Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | DTMB\_CARRIER\_3780 |
| W | 0x00000001 | DTMB\_CARRIER\_1 |
| 1~31 |  | Reserved | -- |

**0x694 - HALREG\_DTMB\_SYNCFRAME:** DTMB Sync Frame Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | DTMB\_SYNC\_420 |
| W | 0x00000001 | DTMB\_SYNC\_945 |
| W | 0x00000002 | DTMB\_SYNC\_595 |
| 2~31 |  | Reserved | -- |

### 6.7 ISDB-T Settings

**0x690 - HALREG\_ISDB\_T\_CONSTELLATION:** ISDB-T Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_DQPSK |
| W | 0x00000001 | ISDB\_T\_QPSK |
| W | 0x00000002 | ISDB\_T\_QAM16 |
| W | 0x00000003 | ISDB\_T\_QAM64 |
| 2~31 |  | Reserved | -- |

**0x691 - HALREG\_ISDB\_T\_FFT:** ISDB-T Carrier Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_FFT2K |
| W | 0x00000001 | ISDB\_T\_FFT8K |
| W | 0x00000002 | ISDB\_T\_FFT4K |
| 2~31 |  | Reserved | -- |

**0x692 - HALREG\_ISDB\_T\_GUARDINTERVAL:** ISDB-T Guard Interval Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_GI\_1\_32 |
| W | 0x00000001 | ISDB\_T\_GI\_1\_16 |
| W | 0x00000002 | ISDB\_T\_GI\_1\_8 |
| W | 0x00000003 | ISDB\_T\_GI\_1\_4 |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_ISDB\_T\_CODERATE:** ISDB-T Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | ISDB\_T\_CODERATE\_1\_2 |
| W | 0x00000001 | ISDB\_T\_CODERATE\_2\_3 |
| W | 0x00000002 | ISDB\_T\_CODERATE\_3\_4 |
| W | 0x00000003 | ISDB\_T\_CODERATE\_5\_6 |
| W | 0x00000004 | ISDB\_T\_CODERATE\_7\_8 |
| 3~31 |  | Reserved | -- |

**0x694 - HALREG\_ISDB\_T\_TIME\_INTERLEAVED:** ISDB-T Time Interleave Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | ISDB\_T\_TI\_DISABLE |
| W | 0x00000001 | ISDB\_T\_TI\_MODE1 |
| W | 0x00000002 | ISDB\_T\_TI\_MODE2 |
| W | 0x00000003 | ISDB\_T\_TI\_MODE3 |
| 2~31 |  | Reserved | -- |

### 6.8 J83.C Settings

**0x690 - HALREG\_J83C\_CONSTELLATION:** J83.C Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | Reserved |  |
| 1 | W | 0x00000002 | J83C\_QAM64 |
| 2 | W | 0x00000004 | J83C\_QAM256 |
| 3~31 |  | Reserved | -- |

### 6.9 DVB-T2 Settings

**0x691 - HALREG\_DVB\_T2\_FLAGS:** DVB-T2 Control Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000001 | T2EN\_EXTEND\_CARRIER\_MODE |
| 1 | W | 0x00000002 | T2EN\_CONSTELLATION\_ROTATION |
| 2 | W | 0x00000004 | T2EN\_INPUT\_TS\_HEM |
| 3 | W | 0x00000008 | T2EN\_DELETE\_NULL\_PACKET |
| 4 | W | 0x00000010 | T2EN\_VBR\_CODING |
| 5 | W | 0x00000020 | T2EN\_TIME\_INTERVAL |
| 6~31 |  | Reserved | -- |

**0x692 - HALREG\_DVB\_T2\_ISSY:** DVB-T2 ISSY Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~1 | W | 0x00000000 | T2\_ISSY\_DISABLE |
| W | 0x00000002 | T2\_ISSY\_SHORT |
| W | 0x00000003 | T2\_ISSY\_LONG |
| 2~31 |  | Reserved | -- |

**0x693 - HALREG\_DVB\_T2\_NIT:** DVB-T2 NIT Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | T2\_NTI\_DISABLE |
| 1~31 |  | Reserved | -- |

**0x694 - HALREG\_DVB\_T2\_L1\_CONSTELLATION:** DVB-T2 L1 Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_L1\_BPSK |
| W | 0x00000001 | T2\_L1\_QPSK |
| W | 0x00000002 | T2\_L1\_QAM16 |
| W | 0x00000003 | T2\_L1\_QAM64 |
| 3~31 |  | Reserved | -- |

**0x695 - HALREG\_DVB\_T2\_PLP\_CONSTELLATION:** DVB-T2 PLP Constellation Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_PLP\_QPSK |
| W | 0x00000001 | T2\_PLP\_QAM16 |
| W | 0x00000002 | T2\_PLP\_QAM64 |
| W | 0x00000003 | T2\_PLP\_QAM256 |
| 3~31 |  | Reserved | -- |

**0x696 - HALREG\_DVB\_T2\_FFT:** DVB-T2 Carrier Mode Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_FFT\_1K |
| W | 0x00000001 | T2\_FFT\_2K |
| W | 0x00000002 | T2\_FFT\_4K |
| W | 0x00000003 | T2\_FFT\_8K |
| W | 0x00000004 | T2\_FFT\_16K |
| W | 0x00000005 | T2\_FFT\_32K |
| 3~31 |  | Reserved | -- |

**0x697 - HALREG\_DVB\_T2\_CODERATE:** DVB-T2 Code Rate Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_CODERATE\_1\_2 |
| W | 0x00000001 | T2\_CODERATE\_3\_5 |
| W | 0x00000002 | T2\_CODERATE\_2\_3 |
| W | 0x00000003 | T2\_CODERATE\_3\_4 |
| W | 0x00000004 | T2\_CODERATE\_4\_5 |
| W | 0x00000005 | T2\_CODERATE\_5\_6 |
| W | 0x00000006 | T2\_CODERATE\_1\_3 |
| W | 0x00000007 | T2\_CODERATE\_2\_5 |
| 3~31 |  | Reserved | -- |

**0x698 - HALREG\_DVB\_T2\_GUARDINTERVAL:** DVB-T2 Guard Interval Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_GI\_1\_32 |
| W | 0x00000001 | T2\_GI\_1\_16 |
| W | 0x00000002 | T2\_GI\_1\_8 |
| W | 0x00000003 | T2\_GI\_1\_4 |
| W | 0x00000004 | T2\_GI\_1\_128 |
| W | 0x00000005 | T2\_GI\_19\_128 |
| W | 0x00000006 | T2\_GI\_19\_256 |
| 3~31 |  | Reserved | -- |

**0x699 - HALREG\_DVB\_T2\_PILOTPATTERN:** DVB-T2 Pilot Pattern Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0~2 | W | 0x00000000 | T2\_PP\_1 |
| W | 0x00000001 | T2\_PP\_2 |
| W | 0x00000002 | T2\_PP\_3 |
| W | 0x00000003 | T2\_PP\_4 |
| W | 0x00000004 | T2\_PP\_5 |
| W | 0x00000005 | T2\_PP\_6 |
| W | 0x00000006 | T2\_PP\_7 |
| W | 0x00000007 | T2\_PP\_8 |
| 3~31 |  | Reserved | -- |

**0x69A - HALREG\_DVB\_T2\_FECTYPE:** DVB-T2 FEC Frame Length Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W | 0x00000000 | T2\_FEC\_16200 |
| W | 0x00000001 | T2\_FEC\_64800 |
| 1~31 |  | Reserved | -- |

## 7. Transform Relate Register

### 7.1 General Register

**0x600 - HALREG\_TRANSFORM\_CNTL:** Transform Control

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0 | W/R | 0x00000001 | BASE\_CMD\_START |
| 1 | W/R | 0x00000002 | BASE\_CMD\_STOP |
| 2 | W/R | 0x00000004 | BASE\_CMD\_TEST\_START\_SINE |
| 3 | W/R | 0x00000008 | BASE\_CMD\_TEST\_START |
| 4-7 | -- | Reserved | Reserved |
| 8 | W/R | 0x00000100 | BC\_REBOOT |
| 9 | W/R | 0x00000200 | BC\_REBOOT\_RESCUE |
| 10-11 | -- | Reserved | Reserved |
| 12 | W/R | 0x00001000 | BC\_RFMIXER\_START |
| 13 | W/R | 0x00002000 | BC\_RFMIXER\_STOP |
| 14-30 | -- | Reserved | Reserved |

\*type W/R register: The register will be cleared after commend executed.

**Description**

* BASE\_CMD\_START: service start command.
* BASE\_CMD\_STOP: service stop command.
* BASE\_CMD\_TEST\_START\_SINE: use sine wave starting.
* BASE\_CMD\_TEST\_START: test mode start.
* BASE\_CMD\_REBOOT: software reset command using with BASE\_CMD\_REBOOT\_RESCURE, if user want to reset chip by software reset, can using this command without chip fail.
* BASE\_CMD\_REBOOT\_RESCURE: software reset command using with BASE\_CMD\_REBOOT, if user want to reset chip by software reset, can using this command without chip fail.
* RFMIXER\_CMD\_START: RF start command, control by VATek chip.
* RFMIXER\_CMD\_STOP: RF start command, control by VATek chip.

### 7.2 RF Mixer Registers

**0x1200 - HALREG\_RF\_COM\_STATUS:** R2 RF MIXER Status Register

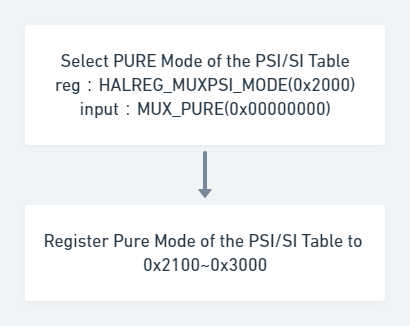
|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0-1 | R | 0x00000001 | RF\_STATUS\_IDLE |
| R | 0x00000002 | RF\_STATUS\_ACTIVE |
| 2-30 | -- | Reserved | Reserved |
| 31 | R | 0x80000000 | RF\_STATUS\_FAIL |

**0x1202 - HALREG\_RF\_COM\_FREQ:** R2 RF MIXER Frequency Register

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit #** | **Type** | **Value** | **Name** |
| 0-31 | W/R | -- | Write desired Frequency (Mhz).   * Frequency minimum step is 1 MHz * Frequency Range from 50Mhz ~ 950MHz |

## Appendix

### A. Register PSI/SI table by using PSI PURE mode

Register table during 0x2100 to 0x3000，refer 5.2。

**一張含有 桌 的圖片

自動產生的描述**

PSITABLE\_REGISTER() {

for (i=0; i<Table\_Number; i++) {

RAWPSI\_EN\_TAG

HALOF\_RAWPSI\_INTERVAL

HALOF\_RAWPSI\_PACKETS

HALOF\_RAWPSI\_DATA

}

RAWPSI\_EN\_ENDTAG

}

32

32

32

32\*N

32

Bits

32

32

32

32

32

Syntax

32

32

32

32

32

Table\_Number: number of register PSI/SI table，16 is maximum。

RAWPSI\_EN\_TAG: start tag when registering PSI/SI table。

HALOF\_RAWPSI\_INTERVAL: interval of transport table。

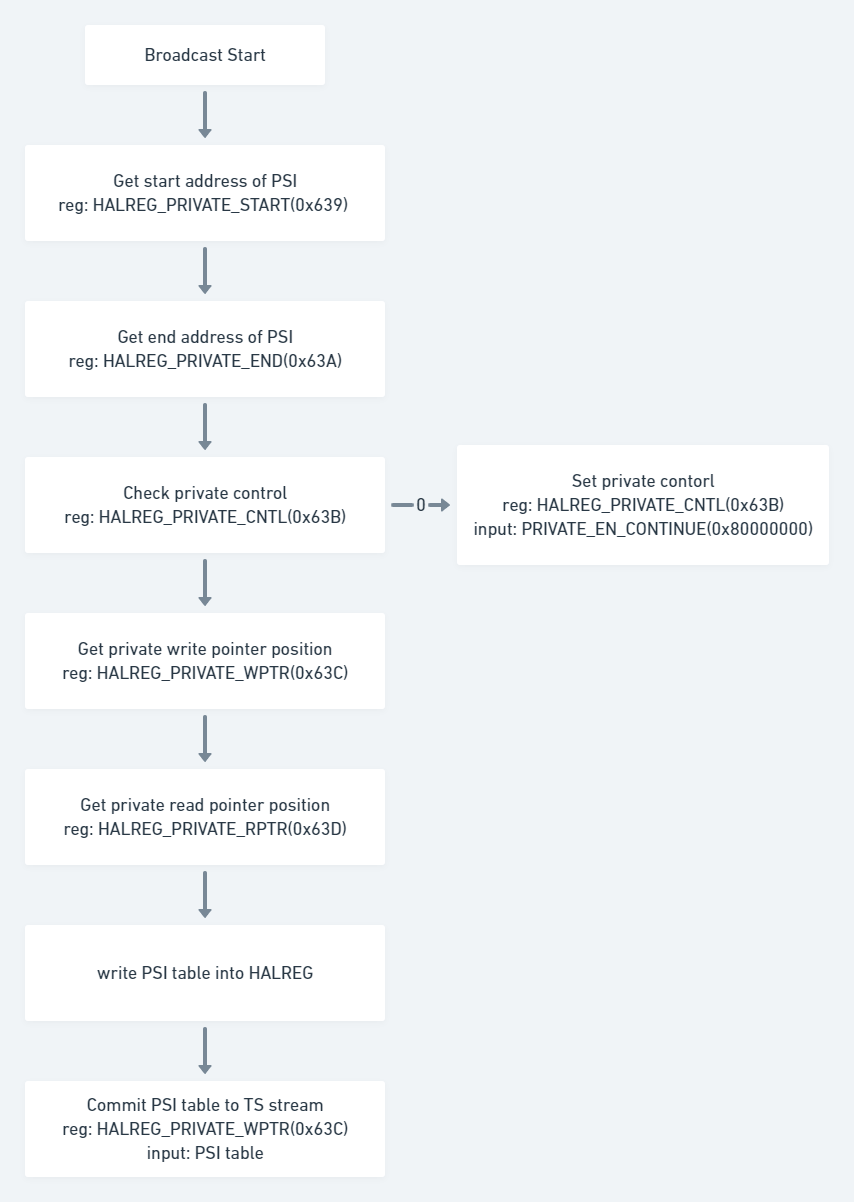
HALOF\_RAWPSI\_PACKETS: packet number of PSI/SI table，each packet max is 188 Bytes。

HALOF\_RAWPSI\_DATA: data of register PSI/SI。

RAWPSI\_EN\_ENDTAG: end tag of register PSI/SI。

### B. Insert PSI/SI table by using PSI PURE mode

Insert table during 0x2100 to 0x3000, refer 5.3



### C. RF start flow (for VATek R2)

